

CLAIMS

We claim:

1 1. A method of extracting electrical characteristics from an integrated
2 circuit layout, said method comprising:
3 dividing said integrated circuit layout into at least one extraction sub problem;
4 identifying a set of physical parameters that define said extraction sub problem
5 from said integrated circuit layout;
6 supplying said set of physical parameters to a machine-learning model trained
7 with Bayesian inference implemented with a Monte Carlo method; and
8 calculating at least one electrical characteristic for said extraction sub problem by
9 analyzing said set of physical parameters with said machine-learning model
10 trained with Bayesian inference implemented with a Monte Carlo method.

1 2. The method as claimed in claim 1 wherein said electrical
2 characteristic comprises capacitance.

1 3. The method as claimed in claim 1 wherein said electrical
2 characteristic comprises resistance.

1 4. The method as claimed in claim 1 wherein said extraction sub
2 problem comprises a net.

1 5. The method as claimed in claim 1 wherein said extraction sub
2 problem comprises a section of interconnect wiring.

1 6. The method as claimed in claim 1 wherein one of said set of
2 physical parameters comprises a distance between a pair of interconnect lines.

1 7. The method as claimed in claim 1 wherein one of said set of
2 physical parameters comprises a wire width.

1 8. The method as claimed in claim 1 wherein one of said set of
2 physical parameters comprises a wire length.

1 9. The method as claimed in claim 1, said method further comprising:
2 selecting said machine-learning model from a plurality of machine-learning
3 models.

1 10. The method as claimed in claim 1 wherein calculating at least one
2 electrical characteristic for said extraction sub problem comprises:
3 determining a capacitance per unit length for a subsection of interconnect wiring;
4 and
5 multiplying said capacitance per unit length by a length of said subsection of
6 interconnect wiring.

1 11. A computer readable medium, said computer readable medium
2 comprising an arranged set of computer instructions for:
3 dividing an integrated circuit layout into at least one extraction sub problem;
4 identifying a set of physical parameters that define said extraction sub problem
5 from said integrated circuit layout;
6 supplying said set of physical parameters to a machine-learning model trained
7 with Bayesian inference implemented with a Monte Carlo method; and
8 calculating at least one electrical characteristic for said extraction sub problem by
9 analyzing said set of physical parameters with said machine-learning model
10 trained with Bayesian inference implemented with a Monte Carlo method.

1 12. The computer readable medium as claimed in claim 11 wherein
2 said electrical characteristic comprises capacitance.

1 13. The computer readable medium as claimed in claim 11 wherein
2 said electrical characteristic comprises resistance.

1 14. The computer readable medium as claimed in claim 11 wherein
2 said extraction sub problem comprises a net.

1 15. The computer readable medium as claimed in claim 11 wherein
2 said extraction sub problem comprises a section of interconnect wiring.

1 16. The computer readable medium as claimed in claim 11 wherein
2 one of said set of physical parameters comprises a distance between a pair of interconnect
3 lines.

1 17. The computer readable medium as claimed in claim 11 wherein
2 one of said set of physical parameters comprises a wire width.

1 18. The method as claimed in claim 1 wherein one of said set of
2 physical parameters comprises a wire length.

1 19. The computer readable medium as claimed in claim 11 wherein
2 said arranged set of computer instructions further perform:
3 selecting said extraction sub problem model from a plurality of extraction sub
4 problem models.

1 20. The computer readable medium as claimed in claim 11 wherein a
2 subset of computer instructions for calculating at least one electrical characteristic for
3 said extraction sub problem perform the follow:
4 determining a capacitance per unit length for a subsection of interconnect wiring;
5 and
6 multiplying said capacitance per unit length by a length of said subsection of
7 interconnect wiring.